

Fig. 1 Performances of LDPC codes generated by semi-random parity check matrixes with $k = 30000$

- $R = 1/3$
- $R = 1/2$
- ▲ $R = 2/3$

Simulation study: Fig. 1 contains the simulated performances of the proposed encoding method for various rates (1/3, 1/2, 2/3) using $\tau = 4$. The decoding algorithm follows that in [2]. The results are essentially the same as those obtained using fully random H.

Conclusion: It has been shown that a semi-random approach to LDPC code design can achieve essentially the same performance as the existing method with considerably reduced complexity.

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Non-binary convolutional codes for turbo coding

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The authors consider the use of non-binary convolutional codes in turbo coding. It is shown that quaternary codes can be advantageous, both from performance and complexity standpoints, but that higher-order codes may not bring further improvement.

Introduction: Turbo codes are error correcting codes with at least two dimensions (i.e. each datum is encoded at least twice). The decoding of turbo codes is based on an iterative procedure using the concept of extrinsic information. Fig. 1 gives an example of a two-dimensional turbo code built from a parallel concatenation of two identical recursive systematic convolutional (RSC) codes with generators 15, 13 (octal notation). The global (non-iterative) decoding of such a code is too complex to be envisaged because of the very large number of states induced by the interleaver. An iterative procedure is therefore used, the two codes being decoded alternately in their own dimensions and the two associated

decoders passing the result of their work to each other, at each iterative step.

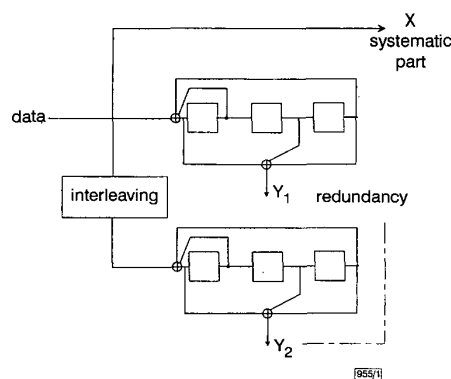


Fig. 1 Two-dimension turbo code with generators 15, 13

Binary codes versus quaternary codes: Fig. 2a represents a block of size k encoded by the code of Fig. 1. This block is seen as a two-dimensional $\sqrt{k} \times \sqrt{k}$ block and for simplicity we consider that the interleaver is a regular one: the sequence is encoded first by C_1 , following the horizontal or line-wise dimension, and secondly by C_2 , following the vertical or column-wise dimension. The dashes on both dimensions symbolise the path error packets at the output of the two decoders, at a particular step of the iterative process. These packets do not contain only erroneous decisions but they indicate where a wrong path has been chosen either by the decoder of C_1 or by the decoder of C_2 . This corresponds to a certain path error density per dimension, which is the same in both dimensions if the component codes are identical.

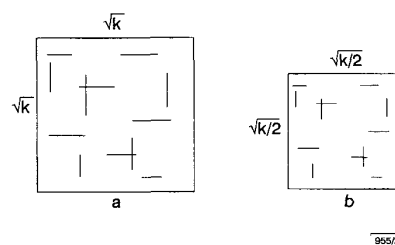


Fig. 2 Path error packets in turbo decoding

- a Binary codes
- b Quaternary codes

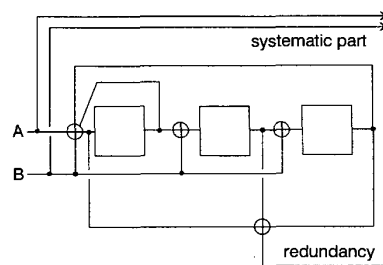


Fig. 3 8-state quaternary recursive systematic convolutional (RSC) code with generators 15, 13

The performance of turbo decoding is strongly dependent on the path error density per dimension. Obviously, the more numerous and the longer the horizontal and vertical dashes in the square box are, the harder the convergence to the correct codeword is. Now for each component code, replace the binary code of Fig. 1 by the quaternary code of Fig. 3. The data are thus encoded and interleaved in couples. The size of the block is $k/2$ couples and the square box now has the dimensions $\sqrt{k/2} \times \sqrt{k/2}$ (Fig. 2b). When a decoder selects a path in the decoding trellis, the same amount of information is used in the cases of both binary and quaternary codes, therefore with half the number of transitions in the case of a quaternary code, giving path error packets which are half the

length. Recalling that each dimension of the square block has been divided by $\sqrt{2}$ and not by 2, the path error density per dimension has been divided by $\sqrt{2}$. This leads to slightly better performance, which was already reported in [1], even in comparison with 16-state turbo codes, which are the reference for practical turbo codes (see for instance [2]).

Table 1: Comparison of computation needs in a 16-state/2-path decoder and in an 8-state/4-path decoder

	16-state/2-path	8-state/4-path
Transition metrics to compute	4	16
Node metrics memory	16 registers	8 registers
Adders for the computation of node metrics	32	32
Comparators for the selection of node metrics	16	24
Adders for the computation of the soft-output	32	32
Comparators for the computation of the soft-output	30	28

Complexity standpoint: Table 1 compares succinctly the combinatory decoding complexity of a 16-state, 2-path per node decoder and that of a 8-state, 4-path per node decoder, corresponding to the code of Fig. 3 for instance. The decoding algorithm considered is the max-log-APP algorithm, also called dual Viterbi decoder [3], whose complexity is roughly twice the complexity of the Viterbi algorithm. Only one processor for forward and backward recursions is considered, but the comparison is still valid. Finally, coding rates for component codes are assumed to be equal to or greater than 1/2. On a first reading, the complexity appears to be of the same order for decoding a binary soft-output in a 16-state trellis and a quaternary soft-output in a 8-state trellis. In fact, taking the size of quantised numbers into account, especially in transition metrics, we can consider that the quaternary decoder is around 30% more complex. If we now refer to the complexity per decoded bit, the quaternary decoder is simpler by 35%. So the conclusion is dependent both on the material support, DSP or ASIC, and on the data rate. However, generally speaking, the 8-state/4-path decoder seems to be more attractive to design. Note also that non-binary decoders have been considered in the literature for a long time for resolving high data rate decoding implementations [4].

Other m-ary codes: Can we extend the principle of quaternary codes to decrease the path error density per dimension to *m*-ary codes with $m > 4$? With quaternary 8-state codes, the shortest wrong path in a decoder is of length 2. Because it is the minimum possible value, increasing *m* is of no interest for this purpose, unless we use codes with more than 8 states. But, unfortunately, the performance of turbo decoding for low signal to noise ratios is debased when adopting large constraint lengths (> 5). This results from the construction of extrinsic information which becomes less and less reliable as the number of states increases. So the relevance of *m*-ary codes ($m > 4$), relatively to the path error densities, would be diminished by some deterioration in the iterative process.

Conclusion: 8-state quaternary codes appear to be good candidates for turbo coding, from the points of view of performance, complexity and throughputs. Encoding data by couples of bits divides the block size by a factor of two. Despite this apparent handicap, the path error density per dimension is lowered, which explains the improvement in performance.

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46GHz bandwidth monolithic InP/InGaAs pin/SBHT photoreceiver

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An InGaAs *pin*-photodetector and a lumped SBHT transimpedance preamplifier have been monolithically integrated and characterised. The preamplifier achieves a transimpedance gain of 44.6dB Ω (170 Ω) and the optical/electrical -3dB bandwidth of the entire receiver is 46GHz, which is the highest bandwidth for any HBT based photoreceiver reported to date.

Introduction: The monolithic integration of photodetectors and preamplifiers in InP-based materials has been the focus of research in industrial and academic laboratories owing to the ease of fabrication. Because the InGaAs base-collector junction of an HBT can be used to form the photodiode, no additional epitaxial and processing steps are necessary for this cointegration. Furthermore, the InGaAs *pin*-diode serves as a detector for light at 1.55 μ m wavelength the interconnection parasitics between diode and preamplifier can be reduced to a minimum, and high-performance transistors are available. Previously, we presented a similar receiver with outstanding results for sensitivity, gain and bandwidth [1]. Our new generation of improved SBHT and a reduction in transimpedance gain to 170 Ω led to the high bandwidth of 46GHz being presented in this Letter. This development step is a consequence of the fact that, with the introduction of Er-doped fibre amplifiers (EDFAs) as optical preamplifiers, the requirements for sensitivity and gain are relaxed and operating speed has become one of the most important issues.

Device structure and fabrication: The self-aligned InP/InGaAs single-hetero junction bipolar-transistor (SBHT) process has been described in detail in [2]. The process provides transistors having an emitter area of $1.0 \times 5 \mu\text{m}^2$, a $9 \mu\text{m}$ diameter photodiode with an antireflection coating, thin-film $50 \Omega/\square$ Cr resistors and supply blocking capacitors formed by base-collector layer depletion capacitances. The MOVPE-grown device layer structure is the same as described in [1] with the exceptions of reduced base- and collector-layer thicknesses of 50 and 400nm, respectively. The latter results from a tradeoff between the collector transit time of the HBT on one side and responsivity, and the parasitic capacitance of the diode on the other side. To extend the RC-limited photodiode bandwidth to well over 40GHz, a preamplifier with low input impedance is necessary. Therefore, we choose a common-base input stage followed by a transimpedance amplifier stage and an emitter-follower output stage (Fig. 1) as originally proposed in [3].

Experimental results: All measurements were performed on-wafer. Optical characterisation was carried out using a lensed singlemode fibre for top illumination. The DC responsivity of the photodiode including coating losses is $R = 0.32 \text{ A/W}$, the parasitic capacitance $C_{\text{dep}} = 70 \text{ fF}$ and the -3dB bandwidth into a 50 Ω load was measured to be $f_{-3\text{dB}} = 30 \text{ GHz}$. The HBTs exhibit a DC current gain of $\beta = 25$, a transit frequency of $f_T = 130 \text{ GHz}$ and a maximum oscillation frequency of $f_{\text{max}} = 270 \text{ GHz}$ at a collector current density of $J_c = 1.3 \text{ mA}/\mu\text{m}^2$ and a collector-emitter voltage range of $V_{ce} = 1.5\text{--}2 \text{ V}$. The DC transimpedance of the preamplifier was measured